L Number	Hits	Search Text	DB	Time stamp
1	1	"6738964" and process$3 same display$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/09 21:31
2	1	"6738964" and process$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/09 21:33
3	1	"6738964" and process$3 and(pin or pins)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/09 21:46
4	1	"6738964" and process$3 and(pin or pins) and (line or lines)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/09 21:51
5	1	"6738964" and process$3 and(pin or pins) and (line or lines) and color$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/06/09 21:51

EAST Browser - L21: (5) oscilloscope... | US 5452239 A | Tag: S,T1 | Doc: 5/5 | Format : KWIC

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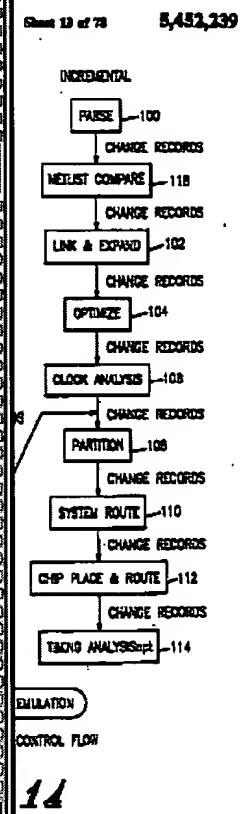
Detailed Description Text - DETX (132):
Turning now to FIG. 12, the multiplexer chip 20 has a large number of bidirectional I/O pins. Any pin can be defined as an input, output, or bidirectional. The chip acts like a large crosspoint switch. Any input can be connected to any output or any group of outputs. It is possible for one input to drive up to half of the other pins on the chip. I/O pins and connection patterns are defined by loading a serial configuration pattern into static RAM inside the chip.

Detailed Description Text - DETX (133):
The chip is statically non-blocking. For any pattern of inputs and outputs, there is a configuration pattern which will make the desired connections. Internally, the chip is a large crosspoint switch where each configuration bit causes a connection between an input pin and an output pin.

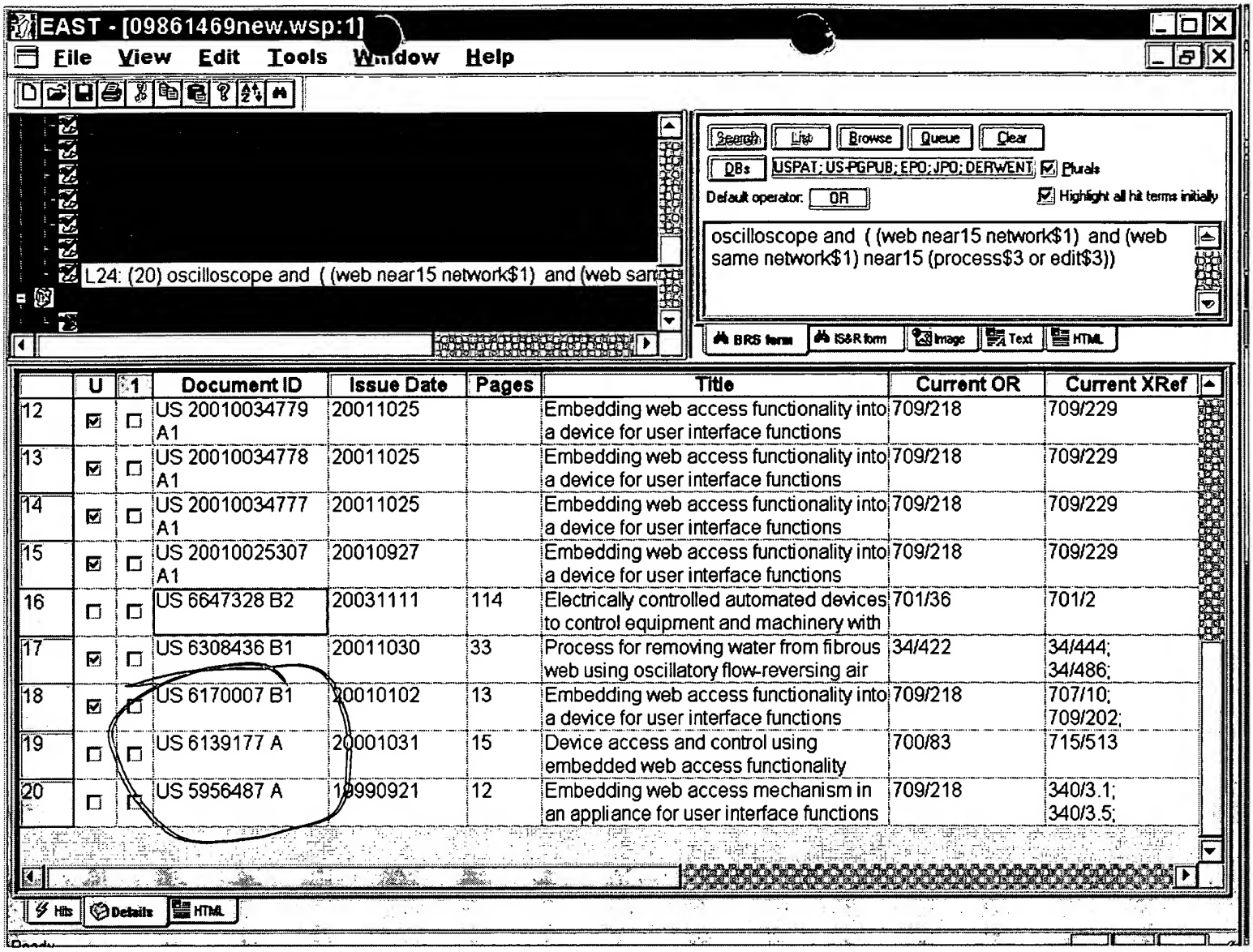
Detailed Description Text - DETX (137):
2. On the Mux Boards 24: Approximately 117 pins connect to other mux chips 20 on emulation modules 16 and 42 pins connect to external component adaptors or pods. Five I/O connectors are available on each mux board, each of which provides 76 I/O signals as well as a subset of the PBUS for programming and testing external devices. Other mux chip pins connect between mux chips or are used to source clock nets as described earlier. CMOS input levels are used for all pins.

Detailed Description Text - DETX (138):
3. On Component Adaptors: 76 Pins connect to the system through the I/O connector. 76 additional pins are available for connection to a user design. These pins can be used in various ways. Up to 38 of them can be bidirectional with separate enables or more if enables can be shared. Up to 76 pins can be static inputs or outputs.

Detailed Description Text - DETX (164):
I/O pins have either 2 or 3 connections to the switching matrix. These are the input, output and output enable. Each output or output enable may be



Details | Text | Image | HTML | KWIC | Full



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
12	☑	☐	US 20010034779 A1	20011025		Embedding web access functionality into a device for user interface functions	709/218	709/229
13	☑	☐	US 20010034778 A1	20011025		Embedding web access functionality into a device for user interface functions	709/218	709/229
14	☑	☐	US 20010034777 A1	20011025		Embedding web access functionality into a device for user interface functions	709/218	709/229
15	☑	☐	US 20010025307 A1	20010927		Embedding web access functionality into a device for user interface functions	709/218	709/229
16	☐	☐	US 6647328 B2	20031111	114	Electrically controlled automated devices to control equipment and machinery with	701/36	701/2
17	☑	☐	US 6308436 B1	20011030	33	Process for removing water from fibrous web using oscillatory flow-reversing air	34/422	34/444; 34/486;
18	☑	☐	US 6170007 B1	20010102	13	Embedding web access functionality into a device for user interface functions	709/218	707/10; 709/202;
19	☐	☐	US 6139177 A	20001031	15	Device access and control using embedded web access functionality	700/83	715/513
20	☐	☐	US 5956487 A	19990921	12	Embedding web access mechanism in an appliance for user interface functions	709/218	340/3.1; 340/3.5;